

1 1. A data storage system wherein a host computer is coupled to a bank of disk  
2 drives through an interface, such interface having a plurality of directors and a  
3 memory interconnected by a four busses, such directors controlling data transfer  
4 between the host computer and the bank of disk drives as such data passes through  
5 the memory, such interface comprising:

6 (A) a printed circuit board having:

7 (a) a plurality of electrical connectors arranged in a linear array and electrically  
8 connected to the busses, such electrical connectors being adapted to receive director  
9 printed circuit boards having the directors and the memory printed circuit boards  
10 having the memory, and electrically interconnect the directors and the memory  
11 received therein to the busses;

12 (b) wherein a front end portion of the directors are coupled between the host  
13 computer and the busses through a front end portion of ESCON adapters and a back  
14 end portion of the directors are coupled between the bank of disk drives and the  
15 busses through the back end portion of the adapters;

16 (c) wherein each one of such adapter boards comprises:

17 (i) a plurality of adapter ports each one being coupled to a corresponding  
18 port of the host computer;

19 (ii) a plurality of adapter board gate arrays;

20 (iii) a plurality of optic interfaces, each one being coupled between a  
21 corresponding one of the adapter port and a corresponding one of the adapter board  
22 gate arrays, wherein each coupled optic interfaces and gate array provides a  
23 corresponding one of a plurality of independent channels for the data, the plurality of  
24 channels being adapted to pass data concurrently therethrough.

1 2. The system recited in claim 1 wherein the memory comprises a plurality of  
2 memory sections each one having different addresses of the memory, each one of  
3 the memory sections being received in a corresponding one of the electrical  
4 connectors and being electrically connected to a corresponding one of a pair of the  
5 four busses, one of the memory sections being electrically connected to a first bus of

6 the first pair of busses and a second bus of the second pair of busses and the other  
7 one of the memory sections being electrically connected to a second bus of the first  
8 pair of busses and a first bus of the second pair of busses.

1 3. The system recited in claim 2 wherein each one of the directors is electrically  
2 connected to the plurality of memory sections through the busses.

1 4. A data storage system wherein a host computer is coupled to a bank of disk  
2 drives through an interface, such interface comprising:  
3 a plurality of directors;  
4 a bus;  
5 a memory connected to the directors through the buss;  
6 wherein the directors control data transfer between the host computer and the  
7 bank of disk drives as such data passes through the memory;  
8 a plurality of ESCON adapters, a front end portion of the directors being  
9 coupled between the host computer and the busses through the ESCON adapters;  
10 wherein each one of such adapters includes:  
11 a plurality of adapter ports each one being coupled to a corresponding port of  
12 the host computer;  
13 a plurality of adapter board gate arrays;  
14 a plurality of optic interfaces, each one of the optic interfaces being coupled  
15 between a corresponding one of the adapter port and a corresponding one of the  
16 adapter board gate arrays, each one of the coupled optic interfaces and gate array  
17 providing a corresponding one of a plurality of channels for the data.

1 5. The system recited in claim 4 wherein each adapter also comprises:

2 a plurality of adapter board CPUs, each one being coupled to the adapter  
3 board gate arrays and the optic interface of a corresponding one of the channels,  
4 each one of the CPUs controlling the initiation and termination of the data passing  
5 through said corresponding one of the channels.

1 6. The system recited in claim 5 wherein each one of the front end portion of the  
2 director boards includes a plurality of director board gate arrays and a  
3 plurality of EDACs; and

4 wherein each pair of the director board gate arrays is coupled between  
5 a corresponding pair of the adapter board gate arrays and a corresponding one of  
6 the EDACs.

1 7. The system recited in claim 6 including a plurality of director board CPUs  
2 each one is coupled to a corresponding one of the adapter board CPUs, each  
3 one of the director board CPUs being coupled to a corresponding one of the  
4 director board gate arrays to control the initiation and termination of a data  
5 transfer through such coupled one of the director gate arrays.

1 8. The system recited in claim 7 including a common state machine coupled to  
2 the plurality of director gate arrays and the plurality of EDACs for arbitrating  
3 between the pair of director gate arrays coupled to the corresponding one of  
4 the EDACs for access to such corresponding one of the EDACs.

1 9. The system recited in claim 8 wherein each one of the directors comprises: a  
2 plurality of dual port RAMs, each one being coupled to a corresponding one  
3 of the EDACs and to at least one of the busses; and, a second common state

